```
"
"  File:        K:\CSCI25~1\VENDING\VendABEL.abl
"  created:     11/07/00 15:37:35
"  from:        'K:\CSCI25~1\VENDING\VendABEL.asf'
"  by:          fsm2hdl - version: 2.0.1.53
"
module vendabel
Title 'vendabel'

Declarations

"clocks
CLK PIN;

"input ports
InThree PIN;
InTwo PIN;
RESET PIN;

"output ports
Output PIN;

"******** SYMBOLIC state machine: Sreg0 ******
Sreg0 STATE_REGISTER;
ConFiveSix, ConFour, ConThree, ConTwo, ConZero STATE;


"diagram ACTIONS

"************* state machine: Sreg0 *************

Equations
" clock signals definitions
        Sreg0.clk = CLK;

State_diagram Sreg0
        SYNC_RESET ConZero : RESET
;


State ConFiveSix:

    IF (InTwo # InThree) THEN
        ConZero WITH
            Output = ^b1;
        ENDWITH
    ELSE  IF (!InTwo & !InThree) THEN
        ConFiveSix WITH
            Output = ^b0;
        ENDWITH;

State ConFour:

    IF (InTwo & !InThree) THEN
        ConFiveSix WITH
            Output = ^b0;
        ENDWITH
    ELSE  IF (!InTwo & InThree) THEN
        ConZero WITH
            Output = ^b1;
        ENDWITH
    ELSE  IF (!InTwo & !InThree) THEN
        ConFour WITH
            Output = ^b0;
        ENDWITH;


State ConThree:

    IF (InTwo # InThree) THEN
        ConFiveSix WITH
            Output = ^b0;
        ENDWITH
    ELSE  IF (!InTwo & !InThree) THEN
        ConThree WITH
            Output = ^b0;
        ENDWITH;


State ConTwo:

    IF (InTwo & !InThree) THEN
        ConFour WITH
            Output = ^b0;
        ENDWITH
    ELSE  IF (!InTwo & InThree) THEN
        ConFiveSix WITH
            Output = ^b0;
        ENDWITH
    ELSE  IF (!InTwo & !InThree) THEN
        ConTwo WITH
            Output = ^b0;
        ENDWITH;


State ConZero:

    IF (InTwo & !InThree) THEN
        ConTwo WITH
            Output = ^b0;
        ENDWITH
    ELSE  IF (!InTwo & InThree) THEN
        ConThree WITH
            Output = ^b0;
        ENDWITH
    ELSE  IF (!InTwo & !InThree) THEN
        ConZero WITH
           Output = ^b0;
        ENDWITH;

" end of state machine - Sreg0


end vendabel
```