CSCI 320  Homework 5 – FSM
Submit all your solutions to Moodle by mid-night on March 2.

1. Design the FSM for the 2-bit binary counter that you built in lab. Your design must use JK flip-flops, and it should include:
   - State diagram
   - State transition table
   - State transition table with binary encodings and JK FF next state designations
   - Next state and output Boolean equations
   - A schematic of the complete state machine

Do not be concerned if the schematic does not match the one in the book as long as the functionality is the same.

2. Design the same 2-bit binary counter in Verilog. Submit your Verilog module.