CSCI 320  Homework 4 – Sequential Logic and Verilog
Submit all your solutions to Moodle by mid-night on Feb 10.

1. Work the following problems from the back of Chapter 3: 53 and 60. You must show your work.

2. For each Verilog module below, sketch (or generate in SynplifyPro) a schematic for the circuit described in that module.

module combo1 (input a, b, c,
               output y);
    assign y = a & b & c | a & b & ~c | a & ~b & c;
endmodule

module combo2 (input a, b, c,
               output y);
    wire a_b, a_c, b_c, a_bOra_c;
    and(a_b, a, b);
    and(a_c, a, c);
    and(b_c, b, c);
    or(a_bOra_c, a_b, a_c);
    or(y, a_bOra_c, b_c);
endmodule

module multiplexer1 (input [3:0] d0, d1,
                     input s,
                     output [3:0] y);
    assign y = s ? d1 : d0;
endmodule