UNCA CSCI 255
Exam 1 Fall 2011

This is a closed book and closed notes exam. Laptops, cell phones, and any other electronic storage or communication devices may not be used during this exam.

Name: Key

If you want partial credit for imperfect answers, explain the reason for your answer!

Problem 1 (30 points) True/False Questions

1. **True** or **False:** The ASCII code is a mapping of characters to numbers.
2. **True** or **False:** Floating point numbers are typically represented in one's complement.
3. **True** or **False:** 2^N is the largest unsigned binary number that can be represented in N bits.
4. **True** or **False:** Ohm's law describes the relationship between current flow through and voltage drop across a resistor.
5. **True** or **False:** The output of a sequential logic circuit is solely a function of its inputs.
6. **True** or **False:** DeMorgan's law states that *A* AND *A* is equivalent to *A*, where *A* is any Boolean expression.
7. **True** or **False:** A Karnaugh map is used to represent the states of a flip-flop.
8. **True** or **False:** An AND gate can be built with fewer transistors than a NAND gate.
9. **True** or **False:** A multiplexer (a.k.a. mux) is a combinational logic device used to select one of many inputs for output.
10. **True** or **False:** Any combinational logic circuit can be build solely with NOT, OR and AND gates.
11. **True** or **False:** *Asynchronous* events are those occurring independently of the system clock.
12. **True** or **False:** A right-shift register is a sequential logic device that could be used to implement division by 2.
13. **True** or **False:** An 8-bit register can be built with 4 flip-flops.
14. **True** or **False:** Combinational logic circuits do not require a clock trigger.
15. **True** or **False:** The clock rate of a system can be set without regard for the combinational logic circuits in the system.

Problem 2 (8 points) Decimal conversion
Convert the following four signed decimal numbers into an eight-bit: (1) unsigned binary representation, followed by (2) two's complement representation.

31	-20
① 0001 1111 ② 0001 1111	① 0001 0100 ② 1110 1100
80	**-31**
① 0101 0000 ② 0101 0000	① 0001 1111 ② 1110 0001

Problem 3 (4 points) Two's complement to hex and decimal conversion
Convert the following two eight-bit two's complement numbers into: (1) hex, and (2) signed decimal representation.

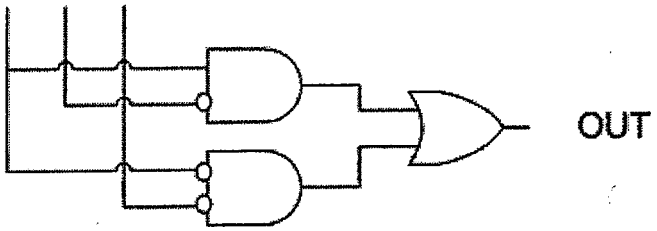
1111|1100	0000|0111
① 0XFC ② 00000100 → absolute value -4 → signed decimal	① 0X07 ② +7 → signed decimal

Problem 4 (12 points) Adding
Add the following pairs of eight-bit two's complement numbers **and indicate which additions result in an overflow.**

00110101 + 10111010 11101111	00100010 + 01101100 10001110 ← overflow
10001010 + 10110110 overflow → 01000000	11101010 + 10101010 110101100

Problem 5 (8 points) Gates to truth
Fill-in the truth table for the gate-level circuit shown below. The three inputs are on the left, the output is on the right.

A B C



$A\bar{B} + \bar{A}\bar{C} = OUT$

A	B	C	OUT
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Problem 6 (6 points) Ranges
How many bits does it take to represent 50 items?

6 bits

What is the greatest number that be represented in 9-bit unsigned notation?

$2^9 - 1$

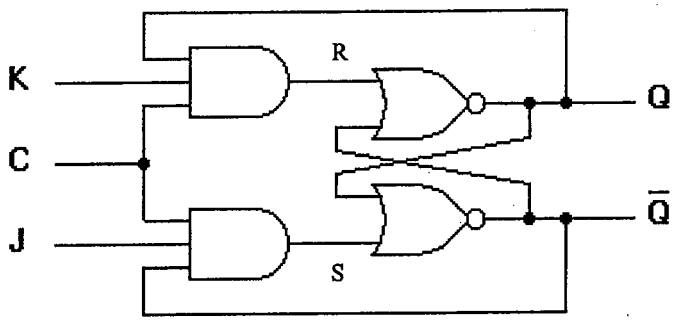
What is the greatest number that can be represented in 9-bit two's complement notation?

$2^8 - 1$

Problem 7 (8 points) JK Flip-Flop
Fill-in the truth table for a JK flip-flop.

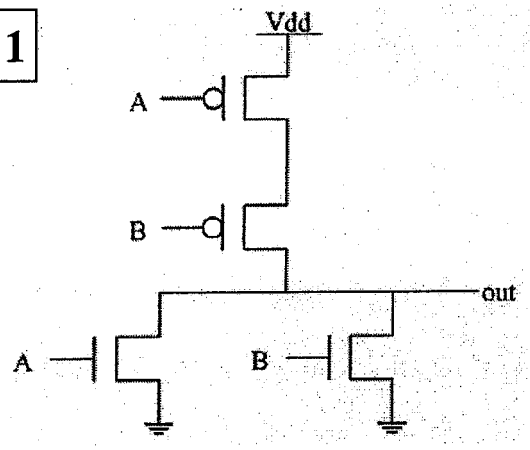
Output: Next State of Q

J	K	Q	Q+	
0	0	0	0	memory
0	0	1	1	
0	1	0	0	reset
0	1	1	0	
1	0	0	1	set
1	0	1	1	
1	1	0	1	toggle
1	1	1	0	

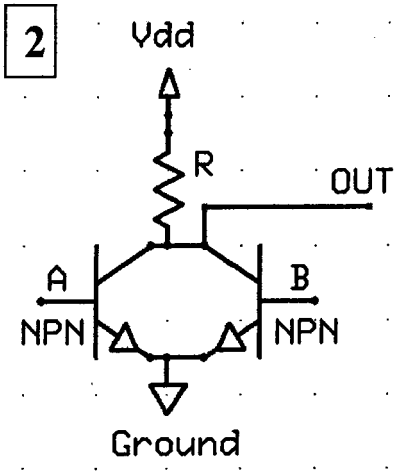


Problem 8 (12 points) Transistors and Circuits
The two circuits below are alternative transistor implementations of the **same logic gate.** In the table below, for each combination of the input values A and B, state the output value and explain how circuit #2 works to produce that output.

1



2



A	B	OUT	Explanation
0	0	1	with the base of both transistors low, there is no connection to ground so OUT = Vdd, i.e. OUT is high
0	1	0	with B high there is a connection to ground so all voltage is dropped across the resistor & out is low
1	0	0	with A high there is a connection to ground through that transistor & all voltage drops across the resistor so OUT= low
1	1	0	same as above except both transistor allows current flow
Name of logic gate:			NOR (a.k.a. NOT OR)

Problem 9 (7 points) Truth to Boolean Expression
Write the Boolean expression that is equivalent to the following truth table, where A, B, and C are inputs and where Z is the single output. You do not need to simplify the expression.

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$Z = f(A,B,C) = \bar{A}\,\bar{B}C + A\bar{B}\bar{C} + ABC$

Problem 10 (5 points) Clocking
For the input and clock signals shown below, provide a timing diagram for the output, Q, of a D flip-flop assuming that the flip-flop is positive edge-triggered.