UNCA CSCI 320
Exam 3 Spring 2014
24 April, 2014

This is a closed book and closed notes exam. It is a 37.5 minute exam to be turned in by 3:00 PM.

Communication with anyone other than the instructor is not allowed during exams. Furthermore, calculators, PDA's, cell phones, and any other electronic or communication devices may not be used during exams.

To ensure compliance with these rules, anyone needing a break during exams must leave their exam with the instructor. The only allowed break excursion is a direct walk to and from the classroom and the restrooms outside RRO 239 (the ATMS classroom). Cell phones or computers may not be used during breaks.

Violation of these rules will result in a grade of 0 for this exam.

Name:_____

This is a 50-point exam.

Problem 1: C/Java floating point to IEEE 754 (10 points)
How is the Java literal 2.25 expressed in 32-bit IEEE 754 format?

You must show your work to get full credit for this problem.

If you need a calculator, you are doing something wrong.

Problem 2 (16 points) Memory caches
Suppose a computer has 16-bit addresses. Show how addresses are broken into tag, set (if any), and block offset fields for a **1 k byte cache** for the following **two** cache structures.

There is a lot of room for figuring below. You must show your work to get full credit for this problem.

Use the 16-bit hexadecimal address `320B` to illustrate your answer.

2A: *An 8-way cache with blocks of size 16 bytes.*

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2B: A fully associative cache with blocks of size 256 bytes.

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By the way, the geometric progression for powers of 2 from 2^0 to 2^9 are:

1	2	4	8	16	32	64	128	256	512

Problem 3 (4 points) Architecture principles
Give a couple of good reasons why RISC processors are unlikely to have an instruction similar to the follow PIC24 instruction.

```
MOV     W5,[++W6]
```

Problem 4 (8 points) SystemVerilog gotchas
Name at least four “features” of SystemVerilog that are likely to trip up an experienced Java or C programmer. Give a reason for each of your choices.

Problem 5 (12 points) Timing diagrams from SystemVerilog
On the left is a SystemVerilog program and on the right is a sequence of `vsim` commands.

```
module jkflipflop(
   input logic clk, j, k,
   output logic q) ;
   always_ff @(posedge clk)
       if (j != k)
         q <= j ;
       else if (j & k)
         q <= ~q ;
endmodule
```

```
force clk 0
force j 1
run 50
force k 0
run 50
force clk 1
run 50
force j 0
run 50
force clk 0
run 50
force k 1
run 50
force clk 1
run 100
```

Draw the wave that would be produced by vsim when executing the SystemVerilog module with the vsim commands. Assume that all four variables have be selected for the wave. You can use the faint grid lines to make your drawing pretty. There may be more lines than you really need.