

**NCSU ECE 109 Sections 602 and 603 and UNCA CSCI 255.001**  
**Exam 2 Spring 2009**  
26 March, 2009

This is a closed book exam. No notes are allowed other than the “handy table” distributed with the exam. Calculators, PDA's, cell phones, and other electronic or communication devices may not be used during this exam.

The exam is to be turned in by 5:45 pm.

Please read and sign the following statement:

I have neither given nor received unauthorized assistance on this test.

Name: \_\_\_\_\_

*If you want partial credit for imperfect answers, explain the reason for your answer!*

**Problem 1 (8 points) Overflow**

Add the following pairs of five-bit two's complement numbers **and indicate which additions result in an overflow.**

$\begin{array}{r} 10000 \\ + 01111 \\ \hline \end{array}$	$\begin{array}{r} 10000 \\ + 10000 \\ \hline \end{array}$
$\begin{array}{r} 11000 \\ + 11111 \\ \hline \end{array}$	$\begin{array}{r} 00011 \\ + 01110 \\ \hline \end{array}$

**Problem 2 (6 points) Decoder and MUX**

If a decoder has 5 inputs, how many outputs does it have?

If a MUX is to select from data 16 inputs, how many selector inputs does it have?

**Problem 3 (12 points) Truth to Gates**

Draw a circuit, at the gate level, that will implement the following truth table, where A, B, and C are inputs and where Z is the single output.

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

**Problem 4 (6 points) Memory**

A computer memory has 16-bit words stored in 2 M locations. What is the size of this memory in bits?

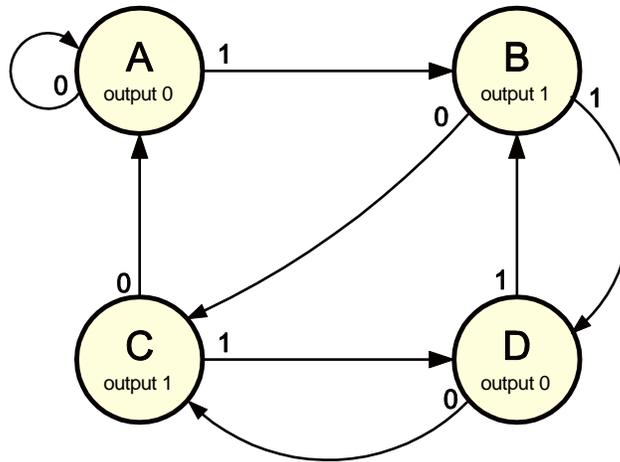
How many address bits are needed to address the 2 M words of this memory?

**Problem 5 (6 points) Data path**

On the first execution cycle of an LC-3 instruction, two operations are performed: (1) the PC is loaded in the MAR, and (2) the PC is incremented by one. Briefly describe how this is done with the textbook's LC-3 data path.

**Problem 6 (15 points) Finite State Machines**

A picture of a finite state machine is given below. The FSM has four states, labeled A to D, and receives single input bit. There is also a single output bit which is shown inside the state. The starting state for the FSM is A.



*Subproblem A:*

Suppose the FSM is started (in state A) and then receives three successive inputs 0 1 1. After the 3<sup>rd</sup> input bit is received, which state is the FSM in and what is its output?

*Subproblem B:*

In the table below give a two-bit state encoding for the four states of the FSM. There are many (actually 24) possible correct answers for this subproblem.

State as letter	State as two bits	
A		
B		
C		
D		

*Subproblem C:*

Complete the following table to show the state transitions of the FSM at the top of the page using your state encodings from the previous subproblem.

<i>present state</i>	<i>input</i>	<i>next state</i>	

**Problem 7 (27 points) Decoding and executing LC-3 instructions**

In this problem, you are going to describe what happens when an LC-3 instruction located at address x4004 is executed. The values of the NZP bits, eight LC-3 registers, and memory locations from x4000 to x4007 when the instruction begins execution are shown below. The memory location for x4004 is vacant because its value varies throughout the problem.

<table border="1"> <tr><td>N</td><td>0</td></tr> <tr><td>Z</td><td>1</td></tr> <tr><td>P</td><td>0</td></tr> </table>	N	0	Z	1	P	0	R0	x0004	M[x4000]	x4004
	N	0								
	Z	1								
	P	0								
R1	x0005	M[x4001]	x4005							
R2	x0006	M[x4002]	x4006							
R3	x0007	M[x4003]	x4007							
R4	x4000	M[x4004]	<i>see below</i>							
R5	x4001	M[x4005]	x0001							
R6	x4002	M[x4006]	x0002							
R7	x4003	M[x4007]	x0003							

Below and on the next page of this exam, there are eleven boxes. In the upper-left corner of each box, there is a 16-bit value. Assume that this 16-bit quantity becomes the value of memory location x4004 and is fetched from memory and executed as an instruction of the LC-3 computer. Within each box, write the result of executing its instruction. Mention every NZP bit, LC-3 register, or memory location changed by the instruction. If the PC is changed by a branch, be sure to mention the updated value for the PC. If the PC is merely increased by one, you do not need to mention that change. If nothing is changed, explicitly say this is the case.

These instructions are *not* executed in order. They are all run *independently* with the register and memory values shown at the top of the page.

The first box has been completed for you as an example. In grading the question, I'll "drop" your score on one of the boxes. (Being generous, I will drop the box where you do the worst.)

Decode all instructions! Even if you aren't sure what the instruction does.

<p><b>0001001010000011</b>  <i>ADD R1,R2,R3.</i>  <i>R1 will be equal to 13 (xC) and the P bit will be set.</i></p>
<p><b>0001001000100011</b></p>
<p><b>0001001000111111</b></p>

0101001111100000
0101010010000010
0000100111111101
0000010000000001
0010011000000001
0110011101000000
1110000000000000
0011011000000010

**Problem 8 (20 points) Decoding and executing an LC-3 program**

In the table below is an LC-3 program that is loaded into five memory locations starting at x3000. First, complete the table by decoding the instructions into the rightmost column of the table.

x3000	0101000000100000	
x3001	0001000000100101	
x3002	0001000000111101	
x3003	0000001111111110	
x3004	1111000000100101	HALT ;TRAP x25

Next, describe the order in which the instructions of this program are executed until it reaches the HALT and give the final values of any registers changed by the program at that time.

Your answer is wrong if (1) it merely repeats the information shown in the table above, (2) there are no instructions that are listed more than once, or (3) you need more room than is available on the remainder of this page.