"Be able to" list for Exam 1

This list is based on Greg Byrd's usual exam review for ECE 109.

Chapter 1

1. Describe the difference between a digital system and an analog system.
2. Describe the sequence of transformations used to solve a problem using a computer.
3. Give one or more examples of each of the following: algorithm, programming language, instruction set architecture, microarchitecture, logic circuit.

Chapter 2

4. Discuss why a binary representation (using 1 and 0) is particularly appropriate for a digital computer.
5. Compute the number of values that can be represented with *n* bits. Compute how many bits are required to represent *k* items.
6. Convert a decimal integer into the following binary representations: unsigned, two's complement.
7. Convert a binary integer to decimal, using the following representations: unsigned, two's complement.
8. Perform two's complement binary arithmetic, and tell whether overflow occurs.
9. Perform the following logic operations on binary numbers: AND, OR, NOT.
10. Convert a character string to ASCII code, and vice versa, given a copy of the ASCII code table.
11. Explain and demonstrate the following concepts: sign extension, overflow.
12. Give two methods for detecting overflow for a two's complement operation.
13. Convert between binary and hexadecimal representations.
14. Convert a decimal number into floating point representation.

Chapter 3

15. Describe the role of the n-type and p-type transistors in a CMOS logic gate.
16. Draw the CMOS implementation of the following gates: NOT, NAND, NOR, AND, OR.
17. Derive the truth table implemented by a given CMOS circuit.
18. Draw the logical symbols used for the following gates: NOT, NAND, NOR, AND, OR.
19. Design a logic circuit that implements a given truth table.
20. Derive the truth table implemented by a given logic circuit.
21. Describe DeMorgan's Law and show its application.
22. Describe the following combinational logic circuits "do": decoder, multiplexer, full adder.
23. Describe the following storage circuits: R-S latch, gated D latch.
24. Discuss the difference between combinational and sequential logic.
25. Given a system description, draw the corresponding state machine.
26. Derive the truth table and design a gate-level implementation of a state machine.

References provided for the exam

If appropriate, you will be given a crib sheet with the following material with your exam.

1. Powers of 2 from 2^{-5} to 2^{10}
2. Hexadecimal digits with corresponding decimal and binary representations
3. Representation of IEEE floating point format (Fig 2.2)
4. Illustration of the implementation of a NAND **or** NOR gate at the transistor level
5. Ridiculously abstract representation of a sequential logic circuit (Fig 3.23)
6. Table of ASCII codes