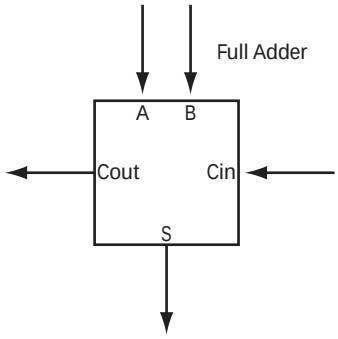
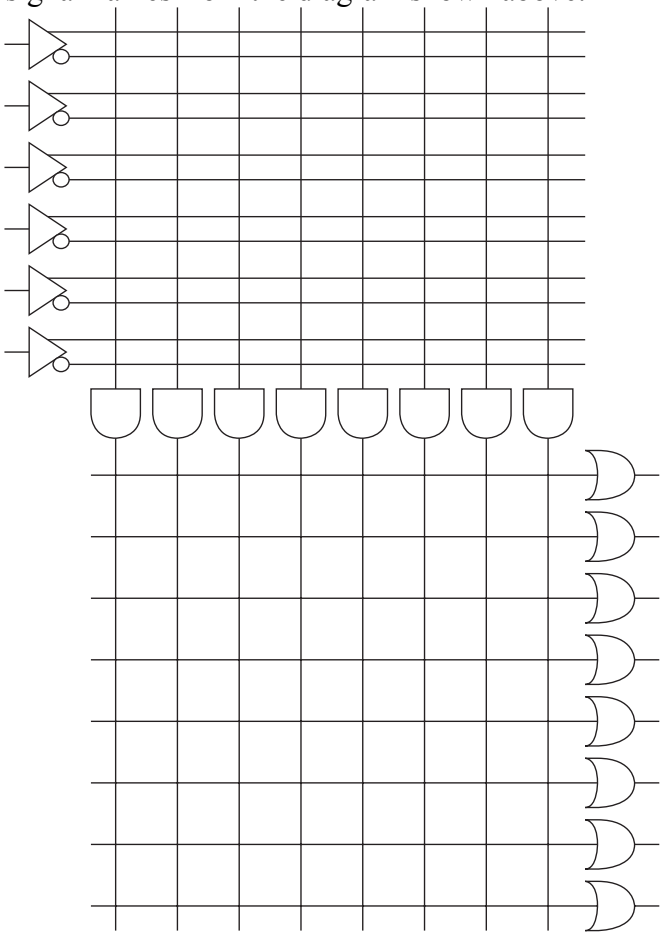
ECE212, Spring 2004

Homework Assignment #5

The block diagram for a 1-bit full adder is shown below.



(1a) Program the PLA below, by marking connections with an "X", to construct a 1-bit full adder. Label PLA inputs and outputs that you use in your solution with the appropriate signal names from the diagram shown above.

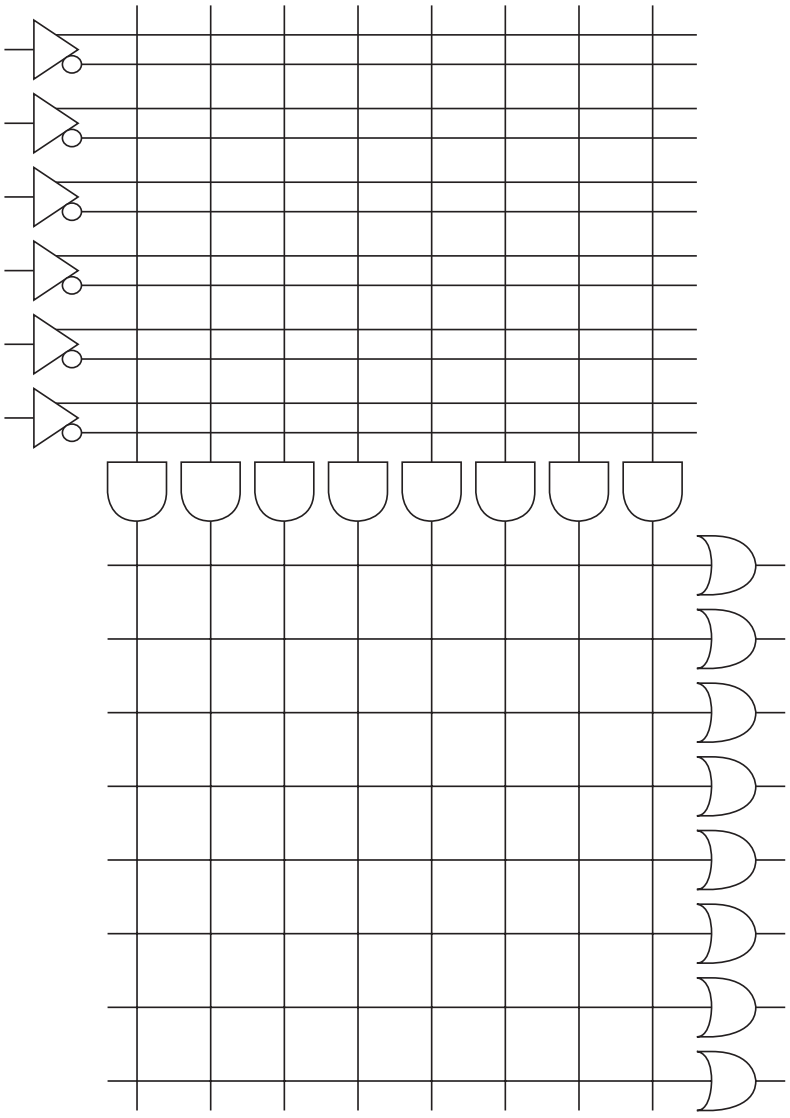


6 x 8 PLA with 8 product terms

(1b) Connect together the required number of full adders to create a 6-bit adder (A5 A4 A3 A2 A1 A0 + B5 B4 B3 B2 B1 B0). In your drawing, use the block diagram shown above, **not the internal PLA implementation**.

(2) Program the PLA below, by marking connections with an "X", to implement a 4-bit even parity generator. The input is a 4-bit word {A3 A2 A1 A0} and the desired output is the parity bit, P. Remember to label the inputs (A3, A2, A1, A0) and output (P) on the PLA.

Hint: You can connect PLA outputs back to PLA inputs to create additional logic levels.



6 x 8 PLA with 8 product terms

(3a) Design a 3-to-8 decoder using discrete logic gates by drawing a circuit diagram. The inputs are C, B, and A, where C is the msb and A is the lsb. The **active-low** outputs are Y0, Y1, … Y7.

Thus, for example, if {C B A} = 100, then Y4 is selected; if {C B A} = 011, then Y3 is selected; and so on. Also include three enable inputs, G1, G2A, and G2B. G1 is **active-high** and G2A and G2B are **active-low**.

(3b) Design a 3-bit 4:1 MUX using discrete logic gates by drawing a circuit diagram. The 4 sources are I0 I1 I2 I3 and the output is Y. Note that these are all 3-bit words. Individual bits of I0 are I0(0), I0(1), and I0(2); individual bits of I1 are I1(0), I1(1), and I1(2); and so on. The select signals are s1 s0, where s1 is the msb and s0 is the lsb

Thus, for example, if {s1 s0} = 10, then source I2 is routed to the output Y; and if {s1 s0} = 01, then source I1 is routed to the output Y.

(4a) Construct a 4-to-16 decoder using only 2-to-4 decoders as building blocks.

The 2-to-4 decoder building block has an **active-low enable** and **active-low outputs**. Label the pins of each 2-to-4 decoder as follows: G is the active-low enable pin, B and A are the input pins where B is the msb and A is the lsb, and Y0 Y1 Y2 Y3 are the active-low output pins. Thus, for example, if {B A} = 10, then output Y2 is selected; if {B A} = 01, then output Y1 is selected; and so on.

For the overall 4-to-16 decoder, label the input signals as N3 N2 N1 N0, where N3 is the msb and N0 is the lsb, and the output signals as DEC0, DEC1, ..., DEC15. Thus, for example, if {N3 N2 N1 N0} = 1000, then DEC8 is selected; if {N3 N2 N1 N0} = 0101, then DEC5 is selected; and so on.

(4b) Construct a 3-bit 8:1 MUX using only 3-bit 2:1 MUXes as building blocks.

For the 8:1 MUX: The 8 sources are I0, I1, ..., I7 and the output is Y. Note that these are all 3-bit words. The select inputs are s2 s1 s0 where s2 is the msb and s0 is the lsb. Thus, for example, if {s2 s1 s0} = 100, then source I4 is routed to the output Y; if {s2 s1 s0} = 011, then source I3 is routed to the output Y; and so on.

(5) Design a 4-bit Comparator which compare the number represented by x3 x2 x1 x0 with the number represented by y3 y2 y1 y0. Output "1" if the numbers are different and "0" if they are the same.

(6a) Design a Parity Generator/Checker to generate **even** parity on 4 bits.

(6b) Explain how an error would be indicated when the data is "checked" with this circuit.