Review Sheet (Exam 2)

You are expected to know the following for the 2nd examination:

- The LC-2 instruction cycle, and how it applies to all the instructions covered in chapter 5.
- Memory organization (i.e. given bit width and number of page bits, determine the number of pages and size of the pages)
- Usage of the LC-2 instructions.
- The addressing modes, and how/which instructions they apply to
- The usage of the condition code registers
- The TRAP instructions (i.e. given a vector, state what the instruction does)
- Given a program, state what the results are
- Given an instruction format, determine how many bits can be used for differing aspects
- The material covered in homework 3
- The material covered on the first test

The following are examples of the types of questions you may see on your test.

1. The following is stored in memory location x3000. Go through the entire instruction cycle, and state the condition of all related registers as they change. 1110 001 100100011
2. A byte addressable memory has a 20-bit address, 8 of which are page bits. What's the size of each page?
3. Create a sequence of instructions that will store R2 – R1 in the memory address located in R3.
4. What is the trap vector for outputting a character to the screen?
5. For problem 10 of chapter 5, state the outcome as well as the results of the condition code registers after each instruction is performed (if any).
6. If the LC-2 only had 4 registers, what is the range for values used as an immediate operand for the ADD instruction?

NOTE: The above are just a sample of the type of information you should know for the test. For example, question 3 uses the base+offset addressing mode, but it could have easily asked for one of the other addressing modes. In addition, a sequence of instructions may require a conditional branch.