CSCI 255, ECE 212, ENGR 274 – Final exam
12 December, 2000

This is a closed book exam. Name: _____
Write all your answers on the exam. To maximize your likelihood of receiving partial credit, **show your work.**

Problem 1. (25 points)
Contrast ten of the following twelve pairs of terms. Cross out the two pair you do not want to be graded. Don't give long definitions of both terms of the pair. Just point out the differences between the two.

a) Open switch – conducts current
Closed switch – does not conduct current

b) Half adder – has two inputs
Full adder – has three inputs

c) Sum of products – OR's together minterms
Product of sums – AND's together maxterms

d) Two level logic network – one level of AND (or OR) gates connecting to another level of OR (or AND) gates
Multilevel logic network – less restricted levels of gates

e) Combinational circuit – has no memory (or time-varying behavior)
Sequential circuit – has memory composed of flip-flops or registers

f) PLA – OR plane connections are not fixed
PAL – OR plane connections are fixed

g) Open collector output – output is driven for one value (typically low) but not the other, generally a pull-up is provided is connect output is driving
Tri-State output – output can either drive low or high or not drive at all (Z)

h) DRAM – dynamic RAM – values "decay" and must be refreshed
SRAM – static RAM – values are held as long as power is present, also a bit faster than DRAM

i) Row address inputs of RAM – high address bits of an address, written to the chip first to select the row
column address inputs of RAM – low address bits of an address, written to the chip to select word within a row

j) Mealy machine – output depends on present state and input
Moore machine – output depends only on present state

k) FPGA – Field Programmable Gate Array – collection of macrocells placed on a chip in a rectangular fashion, interconnection by routing through "streets and avenues", generally specialized from a RAM when powered up
CPLD – Complex Programmable Logic Device – collection of macrocells connected through a central routing network, generally specialized by fuses

l) SR flip-flop – both inputs cannot be one
JK flip-flop – toggles states when both inputs are one

Problem 2. (6 points)
Show how to implement the following functions using one four-to-one multiplexer and some inverters. Draw the multiplexer to the right of the table and show how it would be wired to implement the function.

F(a,b,c) = a' + b' c

a	b	c	a' + b' c	
0	0	0	1	1
0	0	1	1	
0	1	0	1	1
0	1	1	1	
1	0	0	0	c
1	0	1	1	
1	1	0	0	0
1	1	1	0	

Problem 3 (6 points)
Simplify the following two expressions using Boolean manipulation. If you are taking a long time, you are doing something wrong.

a' b + b' a c' + c
=a' b + b' a + c by absorption
(a' b')'
= a + b by de Morgan's

Problem 4 (6 points)
Express the following two numbers in 10-bit twos-complement notation.
-13
= 1111110011
66
= 0001000010

Problem 5 (12 points)

A state table for a finite state machine, where the states are expressed symbolically, is given below:

present state	input	next state	output
A	0	B	0
A	1	A	0
B	0	B	0
B	1	C	1
C	0	B	0
C	1	A	0

In the table shown below, assign binary values to each of the three states.

logical state	binary state
A	00
B	01
C	10

This is one possible assignment – and yes, A and C can be reduced to one state

Suppose you are going to implement this finite state machine with JK flip-flops. Complete the table below using your binary state assignment and showing the values of the inputs to your JK flip-flops. An excitation table for JK flip-flops is given at the bottom of this page.

present state	input	next state	output	flip-flop inputs
00	0	01	0	0- 1-
00	1	00	0	0- 0-
01	0	01	0	0- -0
01	1	10	1	1- -1
10	0	01	0	-1 1-
10	1	00	0	-1 0-
11	0	--	-	
11	0	--	-	

Finally, write Boolean equations for the two inputs to **one** of the flip-flop of your circuit. Hint: choose the flip-flop with the simplest equations.

The simplest flip-flop is the first one. The J input is simply x'y, where x is the first flip-flop and y is the second. The K input is just the constant 1.

old	new	J	K
0	0	0	-
0	1	1	-
1	0	-	1
1	1	-	0

Problem 6 (9 points)
Minimize the following five-state machine by reducing the number of states as much as possible.

present state	input	next state	output
A	0	B	1
A	1	B	0
B	0	E	1
B	1	A	0
C	0	E	1
C	1	A	0
D	0	B	0
D	1	D	0
E	0	C	0
E	1	D	0

In first pass, we group states into two groups by their outputs: {A, B, C} and {D, E}. The first group produces output 1in response to input 0 and output 0 in response to input 1. The second group always produces output 0.

In the second pass, we look at state transitions. The first group, {A, B, C}, can be broken into two groups {A} and {B, C}, because in response to input 1, A goes to an element of group {A, B, C}, while B and C go to an element of group {D, E}.

The three groups are now {A}, {B, C}, {D, E}. Since B and C have the same next states and output, they cannot be separated. Although D goes to B and E goes to C in response to a 0 input, since B and C are in the same group, D and E should not be separated.

present state	input	next state	output
A	0	BC	1
A	1	BC	0
BC	0	DE	1
BC	1	A	0
DE	0	BC	0
DE	1	DE	0

Problem 7 (6 points)
Convert the non-determinate finite state machine given below, where S is the starting state and A is the accepting (1 output) state, into a determinate finite state machine.

present state	input	next state
S	0	S
S	0	T
S	1	S
T	0	A
T	1	T
A	0	A

Start with {S}. In response to 0, {S} goes to {S, T}, and, in response to 1, {S} goes to only {S}.

Now, process {S, T}. This gives transitions to {S, T, A} for 0 and to {S,T} for 1.

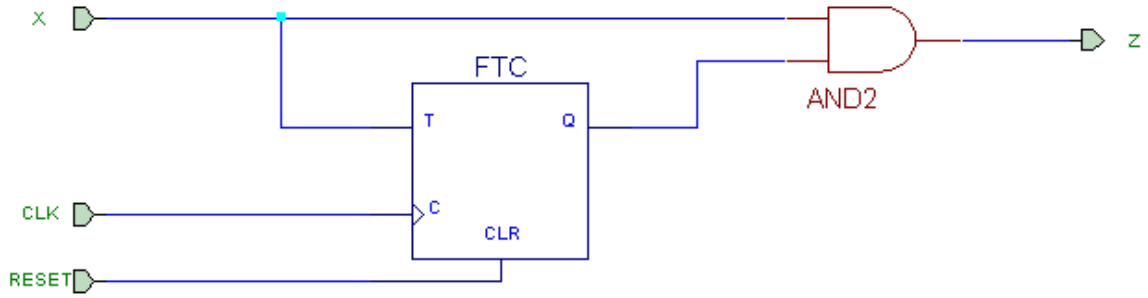
Our new state {S, T, A} goes to {S, T, A} for 0 and to {S, T} for 1.

Here's our state table:

present state	input	next state
S	0	ST
S	1	S
ST	0	STA
ST	1	ST
STA	0	STA
STA	1	ST

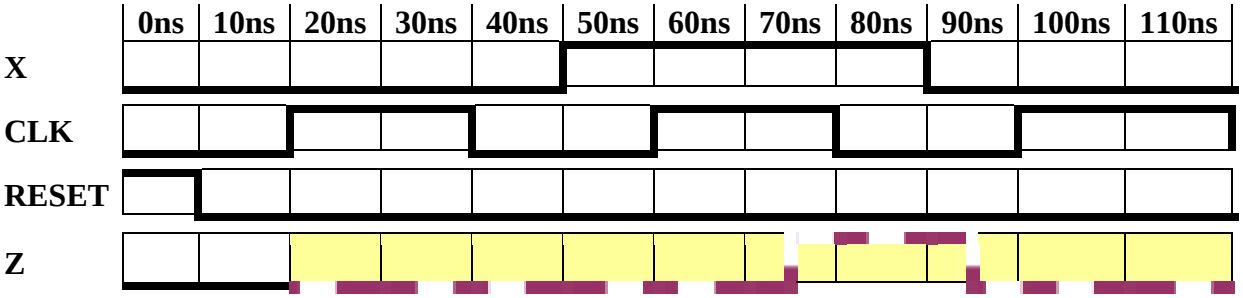
Our new accepting state is STA.

Problem 8 (12 points)
In this problem you will reverse engineer and generate a timing diagram for the following circuit:



The circuit is composed of a *positive edge* triggered T flip-flop and a two-input AND gate. It has a single data input, X, and a single data output, Y. It also has a reset input, RESET, that clears the T flip-flop to 0, and a clock input, CLK. By the way, a T flip-flop *toggles* its output when its input is 1.

Assuming that the T flip-flop has a delay of 10 ns and the AND gate has a delay of 5 ns complete the following timing diagram. Note the RESET is high, and consequently Z is low, at the beginning of the timing diagram.



Now complete the following table, where T is the flip-flop input, and Q is the flip-flop output.

Present state Q	Input X	Flip-flop input -- T	Next state	Output Z
0	0	0	0	0
0	1	1	1	1
1	0	0	1	0
1	1	1	0	0

And finally, draw a state diagram, the one with circles and arrows, for this circuit. Don't worry about figuring out what it does. It does nothing interesting.

You can draw it using the above table…. I didn't in this answer.

Problem 9 (9 points)
In which programming language is the following code written?

```
If RST='1' then
  Trans_count := 0 ;
  MyOut <= '0' ;
```

VHDL

Briefly explain the actions of the three operators with the '=':

a) = Tests for equality of arguments

b) := Assigns to a variable – internal value

c) <= Assigns to a signal – external value

Finally, name a company that manufactures devices that can be programmed with this language.

Xilinx

Problem 10 (9 points)
A finite state machine has two inputs and one output. The output becomes 1 whenever both inputs are 1 and remains 1 until both inputs are 0, as shown in the following table:

Input 1	000**1**1110**0**101**1**01**0**0
Input 2	000**1**0001**0**010**1**10**0**0
Output	000**1**1111**0**000**1**11**0**0

Draw a state diagram for this machine. The number of required states is extremely small.

Sorry, I just can't bring myself to do it. There are only two states.